AIDS FOR DIGITAL IC SYSTEMS*

by Murray Siegel and Lee Marley

INTRODUCTION

When the type of integrated circuit has been chosen, the designer is confronted with the problem of putting them into a finished product. This paper provides the answer with a step-by-step approach to IC utilization.

To take digital building blocks and convert them into an operative subassembly or system is the joint responsibility of the manufacturer and the user. Much effort has been devoted to outlining ease of system design, but little has appeared to help users develop techniques for breadboarding and layout of circuits under study.

Work recently undertaken to fill the void has resulted in the development of "systematic procedures" (Rex Rice, "Systematic Procedures for Digital System Realization from Logic Design to Production," Proceedings of the IEEE; Vol. 52, No. 12; December 1964) for various packages now used for integrated circuit packages (ICP's). These packages are multilead TO-5's (JEDC TO-99 and TO-100) types, Cerpak (flat packages), and Dual-in-Line**modular packages (DIP's). Much remains to be done in helping users reach the most economical finished product design.

This paper outlines the techniques of implementing ICP's. These techniques have been used by Fairchild during logic design projects. Although the outlines are not state-of-the-art, they are indicative of present-day practices that readily can be applied by users who find themselves evaluating ICP's as "the way to go".

CONSTRUCTION AIDS

Assuming a satisfactory logic design has been achieved, the next step is to transform the paper into hardware. This conversion can be simplified by the use of various construction aids, as discussed in the following sections.

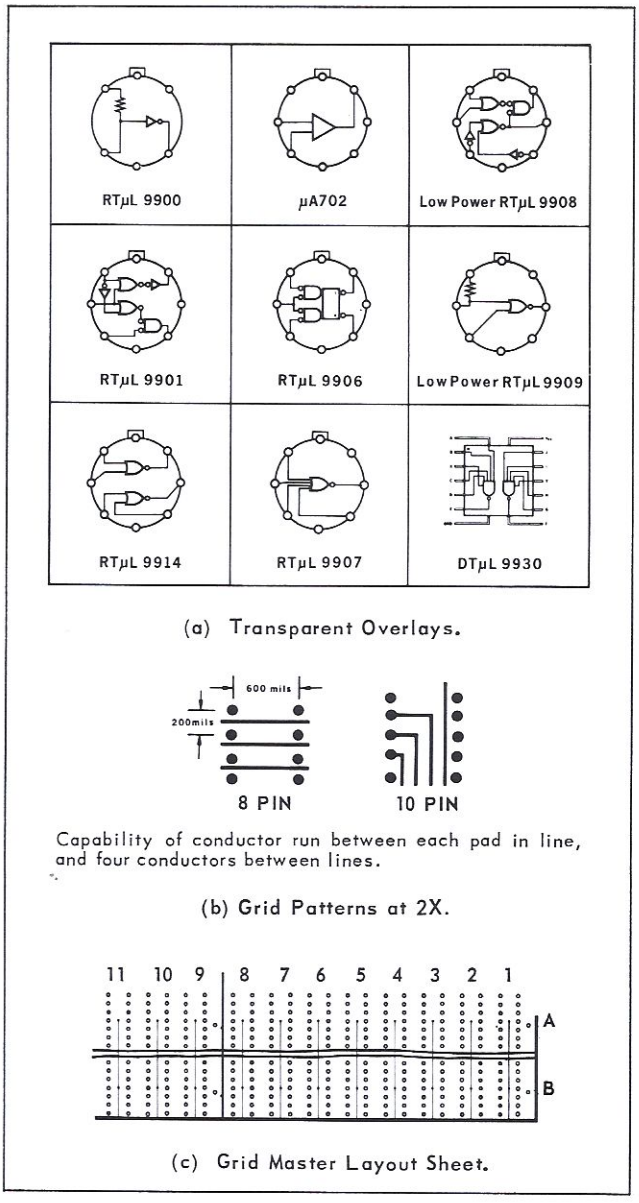

Fig. 1. Samples of Construction Aids.

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**Fairchild patent pending.

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Transparent Overlays

Logic Symbols - To assist designers in the layout of logic blocks, gummed transparent overlays (Fig. 1a) have been designed using Military Standard 806-B "Graphic Symbols for Logic Diagrams" as the basis for all available symbols. The preferred symbol overlay diameter is 0.8 inch. Only where a definition is not available in MIL Standard 806-B would a deviation be made.

If overlays are used, logic layout becomes merely a matter of affixing the desired logic symbols and drawing the data flow lines. The symbols make it easy to check fan-in, fan-out, and delays on the original drawings.

A word about the logic symbols will help clarify their meaning. Look at the symbol for a 9914 gate element in Fig. 1a. The input or output terminals can have one of the two states: "zero" or "one". The zero state refers to an inactive state; the one state is the significant or active state. A small circle or dot at the point where a signal line joins the symbol indicates that the line's active state is the relatively low signal. The absence of such a circle or dot indicates that the line's active state is the relatively high symbol.

Grid Patterns - Other aids can be used in the layout of a given circuit. Fig. 1b shows the configuration for Dual-in-Line grid patterns. Ease of conductor flow between pads is pictured. Gummed transparent overlays of the grid patterns, at 2X, are available from J. Lissner & Sons (see Table I).

In addition, a grid master layout sheet at 2X may be used in the printed-circuit layout. (An example is shown in Fig. 1c.)

Conductor Spacing

Use of available spacing on a printed-circuit card is affected generally by the method of conductor flow. This can be seen by the limitations presented in using the standard pin circle available in a TO-5 package.

8-Lead TO-5's - An 8-lead TO-5 package has a 200-mil pin circle. The center-to-center spacing is 78.5 mils. Using a standard pad size of 50 mils leaves a 28.5-mil clearance between pads. A typical drill hole of 25 mils gives adequate landed area for any of the standard solder techniques.

10-Lead TO-5's - The 10-lead TO-5 package requires a 230-mil pin circle to give the user greater pin-to-pin clearance; however, the center-to-center spacing is reduced to approx-

TABLE I.
CONSTRUCTION AIDS.

SOCKETS

NO. S	COMPANY	LOCATION	TYPE DEVICE	ORDER NO.
1.	Augat	Attleboro, Mass.	14 pin DIP	314 AGIA
2.	Augat	Attleboro, Mass.	16 pin DIP	-
3.	Augat	Attleboro, Mass.	8 pin TO-5	8092-IG5
4.	Augat	Attleboro, Mass.	10 pin TO-5	8092-IG6
5.	Augat	Attleboro, Mass.	14 pin F. P.	8075-IG1
6.	Azmuith	Hanover, N. J.	14 pin F. P.	5100-1
7.	Azmuith	Hanover, N. J.	14 pin F. P.	5106-1
8.	Azmuith	Hanover, N. J.	14 pin F. P.	5107-1
9.	Azmuith	Hanover, N. J.	14 pin F. P.	5108-1
10.	Barnes	Lansdowne, Pa.	16 pins DIP	MGX-27
11.	Barnes	Lansdowne, Pa.	8 pin TO-5	MG-802
12.	Barnes	Lansdowne, Pa.	10 pin TO-5	MG-1002
13.	Barnes	Lansdowne, Pa.	14 pin F. P.	MD-75
14.	Cinch-Jones	Chicago, Ill.	8 pin TO-5	132-38-10-019
15.	Garlock	Cherry Hill, N. J.	14 pin DIP	69013-0528
16.	Garlock	Cherry Hill, N. J.	16 pin DIP	69013-0529
17.	Garlock	Cherry Hill, N. J.	8 pin TO-5	69012-0051
18.	Garlock	Cherry Hill, N. J.	10 pin TO-5	69012-0053
19.	Nugent	New Albany, Ind.	16 pin DIP	EX-780
20.	Nugent	New Albany, Ind.	8 pin TO-5	TP-5178
21.	Nugent	New Albany, Ind.	10 pin TO-5	TP-51710

OVERLAYS

NO. S	COMPANY	LOCATION
1.	Artist Aid J. Lissner & Sons	Los Angeles, Calif.
2.	Engineering & Science Aids	Jersey City, N. J.
3.	Stanpat	Long Island, N. Y.

PC BOARDS

NO. S	COMPANY	LOCATION
1.	ABC Battery Co.	Richland, Wash.
2.	Printex	Mountain View, Calif. Dual-in-Line only
3.	Videx Corp.	Sunnyvale, Calif.

GRID PATTERNS

1.	Artist Aid J. Lissner & Sons	Los Angeles, Calif. (2X)

imately 70 mils. Using the same pad size as above, a pad clearance of 20 mils is available. Thus, runs cannot economically be placed between the leads of a standard TO-5 outline.

Landless, plated-through holes are not required except for military-type users who might desire the advantages of landless plated holes. A cost increase of about 10 percent over landed pads is the penalty.

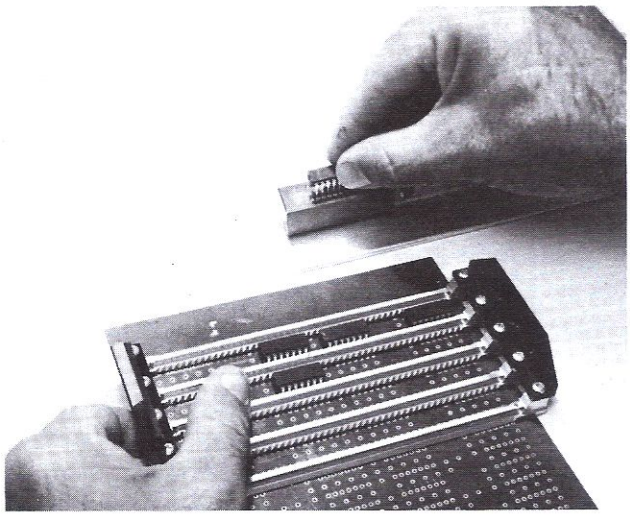

Fig. 2. An Arrangement for ICP High-Speed Hand Insertion.

Dual-In-Line Pattern-As a means of removing the pin circle limitation, the dual-in-line pattern has been adapted, which allows freedom of conductor runs beneath the package. The leads are on centers of 100 mils at 1X, (200 mils at 2X), with 300 mils at 1X (600 mils at 2X) between the rows.

The pads are 3/64 inch at 1X (3/32 inch at 2X) and the tape is 20 to 25 mils at 1X (40 to 50 mils at 2X). Thus, present-day printed-circuit-board technology may be used with these packages. Centers of 100 mils at 1X allow the devices to be used without a drastic limitation on the board manufacturer. Line widths and spacing may be used so that solder bridging is not a drastic problem. Inspection may be made readily. Using printed-circuit line widths and clearances of approximately 20 to 25 mils at 1X, one may run a line between the 100-mil center pins, and up to four lines between rows. Fig. 1b shows how lines may be run between pads.

These Dual-in-Line* package configurations provide advantages in the layout and manufacture of the printed-circuit boards. Obviously, the grid design makes it much easier to tape-program the drilling of printed-circuit boards during manufacturing. For prototype work, either drilling on a milling machine or rapid setup for hand drilling this pattern allows substantial savings in time and effort. In using any pattern, it would be advisable to face all packages in the same direction. There may be cases where it would be advantageous to have some of the packages facing different directions, but often this arrangement has been found to scramble the information flow and increase the complexity of the wiring.

Following a decision to develop the Dual-in-Line package, examination of the methods for maximizing PC density and utility led to innovations in TO-5 insertion and layout techniques, which resulted in the TO-5 packages having the same pin spacing as the DIP.

Insertion Techniques

Insertion of ICP's into a board can be time consuming. A method of staircasing TO-5 leads by cutting them on a diagonal and placing the largest lead into the board first, followed by the rest of the leads in descending order, can cut insertion time. It is the consensus of IC manufacturers such as Fairchild that, in the near future, the Dual-in-Line package will replace the TO-5 package throughout the industry. Toward this end, time has been spent on detailed evaluation of insertion techniques.

The insertion of a TO-5 package into a dual-in-line configuration can be aided by a double staircase with the long lead in one line opposing the shortest lead in the other. Using the 100-mil center-to-center grid results in the device being mounted approximately 250 mils off the board. After soldering, the leads are held firmly in place in a mechanical arrangement. The increased height is normally not a penalty, since interconnection gained by use of connectors dictate the intercard distance with clearance for the ICP's.

Various schemes for both hand-operated and semi-automatic insertion are either in the experimental stages or are already entering the market. Figure 2 shows one scheme for high-speed hand insertion for ICP's, where devices are fed from the shipping magazine to an aligning fixture, which corrects any error of lead position. The package is then placed in the PC board using the guide matrix to locate leads to close-tolerance holes. The guide matrix slides off the board without dislocating the packages. The pin rows are aligned to 325 mils by the jig. As the leads are inserted, the pins

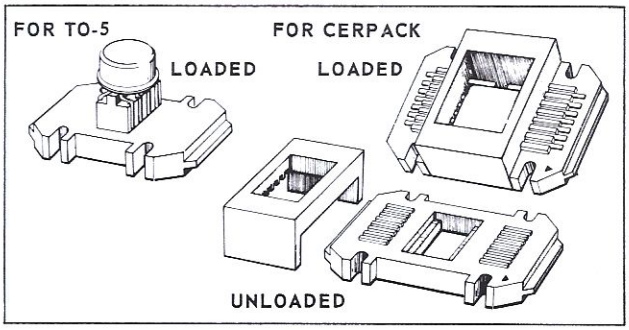

Fig. 3. Integrated-Circuit Carriers.

*Fairchild patent pending.

spring back against the board pattern at 300 mils, which holds the package securely in position.

One means of mechanical insertion being marketed is the DIP Insertion System. * In this system the packages are fed from the magazines, then automatically positioned in the insertion mechanism, and held by outside formers that align the leads. The packages are then inserted, clipped, and clinched. These rapid-insertion capabilities will capitalize on the modular construction of the Dual-in-Line**package, allowing companies in the industrial, commercial, or consumer fields to take advantage of the DIP.

Fairchild has made several types of IC carriers available, since testing and general handling require special consideration. (Examples are shown in Fig. 3.) Manual test fixtures and automatic test-sort fixtures for these carriers are also available.

Breadboards

Because a circuit must first be assembled to be evaluated, it is worthwhile to give serious thought to breadboarding procedures. The number of breadboarding techniques is limited only by the imagination, but a few which have been found to be of general use will be discussed in some detail.

Pin-Circle PC Board-One type of breadboard for TO-5 type packages is a printed-circuit card (Fig. 4) measuring 4 by 5 inches and capable of housing 16 elements. This printed-circuit card is available from two sources (see Table I). The price is about $4 for a two-sided board, which includes approximately 400 pre-drilled holes. There are contacts for a double 22-pin PC connector. The card is glass epoxy using 203 copper runs.

The breadboard pads have provisions for two wiring connections at each lead. V_{CC} and ground are bussed to each pad. No. 26 wire provides a neat and rapid method for interconnections of the various pins. This wire is the thermal strip type, where heat is used to remove insulation from the wire† By making a loop of the inserted TO-5 leads, a convenient test point can be made for scope leads.

This card provides a fairly rapid method of breadboarding some circuit areas. Its greatest drawback may occur when the system will utilize the devices at their maximum speed. In this instance, the wiring may not provide a true demonstration of the final capability of the system.

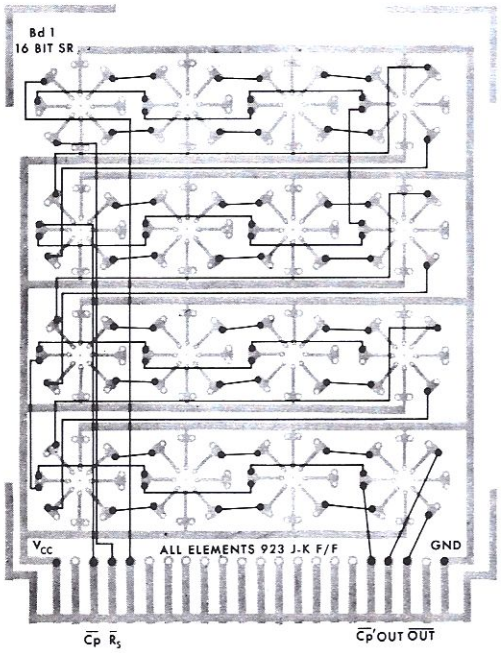

Fig. 4. A PC Board Layout Used As A Wiring Aid and Diagram.

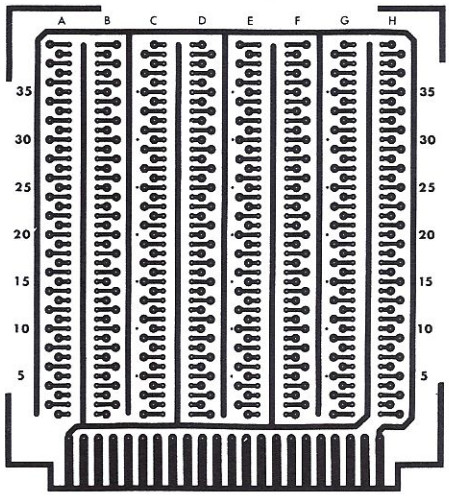

Fig. 5. Popular Type of Breadboard Capable of Housing Both TO-5 and Dual-In-Line Packages.

Dual-in-Line PC Board - Fairchild has designed a second type breadboard configured to a dual-in-line pattern (Figure 5), which is in standard use. Mounting either TO-5 or Dual- in-Line packages or intermingling these packages, both in type and number of leads, on this type card is possible. Up to forty 8-pin TO-5 packages may be wired on the board (in contrast to the total of 16 on the previously described board). Wiring and usable construction aids for the 40-element board are similar to the 16-element board. This printed-circuit card is available from three sources (see Table I). Although each of the sources has slightly modified the board, application-wise the boards are basically the same. The price (from $4. 00) for a two-sided pre-drilled board with over 650 holes depends on the source.

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* Universal Instruments Corp. , East Frederick Street, Binghampton, New York, 13902.

**Fairchild patent pending.

† Available IWI Division of Essex Wire Corporation, 1510 Wall Street, Fort Wayne, Indiana.

Basic Breadboarding Steps - Breadboarding will be simplified if a few basic procedures are followed, as noted below.

1. Give attention to layout, which can be advantageous in following through the circuit during testing.
2. Group all packages as per function.
3. Break the circuit down into boards, controlling your decision by related functions, number of packages, and number of required external inputs and outputs.
4. Gather up partial packages, such as two separated halves of a dual two-input gate.

Wiring Aids - The artwork for the breadboard can be converted into wiring aids and diagrams, as the one shown in Fig. 4. This method proves particularly helpful when the breadboard is given to a fabricator to complete. Because of its large, clear layout, the diagram is also helpful in tracing out the circuitry. Observe that each pad that is interconnected has the circle darkened. The external lines are marked by signal names to tie in with other boards. In this example, all elements are the same, as noted at the bottom of the sheet; whereas in most cases they will differ. When they differ, a simple notation can be made within the circle.

A double entry call-out has been found to be more effective when using the dual-in-line breadboard because of its greater density capability. The vertical rows are numbered from 1 through 40, and the horizontal rows are lettered from A through H. The identification is marked by each pad to show where the connection goes to and/or came from.

Notes and instructions can be put on the wiring diagrams, providing almost complete information for the builder. When wiring is finished, the board can be cleaned by dipping in trichlorethylene (TCE) vapor.

Sources for such items as overlays, grid patterns, sockets, and PC boards, are listed in Table I. Since a great deal has been written on connectors by various manufacturers, they will not be discussed in detail here, other than to say that any major manufacturer of PC connectors should be able to give detailed information.

Other Types of PC Boards - Although similar partial printed-circuit breadboards are available from various manufacturers, they are generally more expensive and have no real advantage over the aforementioned breadboards at this stage of your design.

Another method that may be used is the Vector Board (64 A18).* This is a board with precut holes, where the components are mounted on split stand-offs, with the placement of devices at your discretion. The size of the board is determined by the size of the circuit. External connections are made by leads rather than connectors.

For efficiency and ease, the breadboard shown in Fig. 5 is recommended, but whatever method is used, the next step is the preparation of the printed-circuit board.

PRINTED-CIRCUIT BOARDS

The first and most important step in a printed-circuit board is the layout. The length of time spent in the layout is insignificant compared to the time spent testing and reworking boards made from a poor layout. When density is greater, difficulty in layout and error probability increase proportionately, demanding utmost caution, planning, and checking. Nearly as important is versatility. Use certain basic rules, but do not become tied down strictly to one precise method, as changes are extremely rapid in this field.

Information Flow

The first step in the layout is the positioning of components onto a pad pattern. As with breadboards, it is necessary to be cognizant of the related functions and the number of packages required. But more than this is involved. While there may be several small areas of related functions, there probably will be interweaving of common signals between functions in addition to V_{CC} and ground lines; e. g. clocks, resets, and comparisons between one counter and another. Some minimization of long runs can be minimized to some extent by careful assembling of groupings.

The recommendation is to lay out the remaining long runs before the shorter ones, which prevents being tied down when the work is 75 to 80 percent complete. Not only extremely long and possibly critical lead lengths, but extensive usage of through pins can result. Through pins will increase error probability by the requirement of additional interconnections.

After the longest runs have been considered, the elements with external connections should be located as near the fingers as possible. The component placement should allow the lines to run horizontally on one side of the board and vertically on the other.

Packaging Density Determination

One common question asked is, "How many devices can be packaged in a given area?" Many of the packaging applications are on a 4-1/2 by 5 inch card, hence the answer will be given in these terms. If 25 to 35 ICP's with interconnecting wiring can be put on a board (assuming a general logic configuration), we feel that we have done very well. This is strongly influenced by the amount of interconnecting wiring

*Built by Vector Manufacturing, Los Angeles, California.

needed. In one application, 64 J-K flip-flops, four buffer elements, and four inverters were placed on a single 4-1/2 by 5 inch board. In this case, the interconnecting wiring was obviously very simple, enabling packaging of 72 cans on a board this size. However, as more complex functions are incorporated within a given package, much greater functional density rapidly becomes a practicality.

This particular example could be further reduced in size with the advent of dual RTμL and the four-bit shift-register elements.

Layout Sheet

After a grid pattern is determined and the preliminary grouping of the circuit components has been completed, a wiring layout sheet is made to interconnect all points. Rather than using a separate sheet for each side of the board, and having to alternate from one sheet to the other, a single sheet with a different color representing each side of the board is recommended. The layout is done on a 2X scale using dots to indicate pads. Fig. 6 is an example of a printed-circuit layout sheet and represents sections of a circuit. The resulting board will be referred to again as we follow through the procedure. Random notes may be made on the layout sheet to assist the layout. The material for the layout sheet may be either Clearprint vellum*(No. 1000H010) or K&E "Mylar" Phenix tracing cloth (N-166).*

*Clearprint Paper Company, San Francisco, California, and Keuffel & Esser, Hoboken, New Jersey, respectively.

Line Runs

In laying out the lines, use the same information flow pattern determined during package location. Minimize long runs, use the shortest possible lines for external connections, and tie in group by group. As you proceed, you may be able to make slight alterations. Lay the lines as close together as tolerances permit, since the total picture of all lines required will not be available until the circuit layout is nearly complete. Then the lines may be placed to give optimum spacing and appearance. In going to the other side of the board, wherever possible use the pads for the package leads rather than using through pins. A pin on a package that is not connected internally or the pads on the connector may occasionally be used to advantage.

A discrete intermingling of horizontal and vertical lines, keeping one side basically horizontal and the other side basically vertical, has proved to be a less complex layout. Also, this arrangement is easier to follow in testing than strict adherence to horizontal and vertical sides. The user's application will determine which is best. A good example of this is the case where, in a particular circuit of 40 packages, discrete intermingling eliminated 88 through pins on the ground line alone. A method of running V_{CC} and ground lines with a minimum hampering of information flow is shown in Fig. 7. Use the two outside pins on the external connection for V_{CC} and ground. One line goes above the devices, the other below, forming an interlocking finger-like pattern. This becomes the basically horizontal side. Tape widths from a minimum of 40 mils at 1X (80 mils at 2X) to a normal maximum of 60 mils at 1X(120 mils at 2X) are recommended when the boards have 100-mil centers for V_{CC} and ground busses.

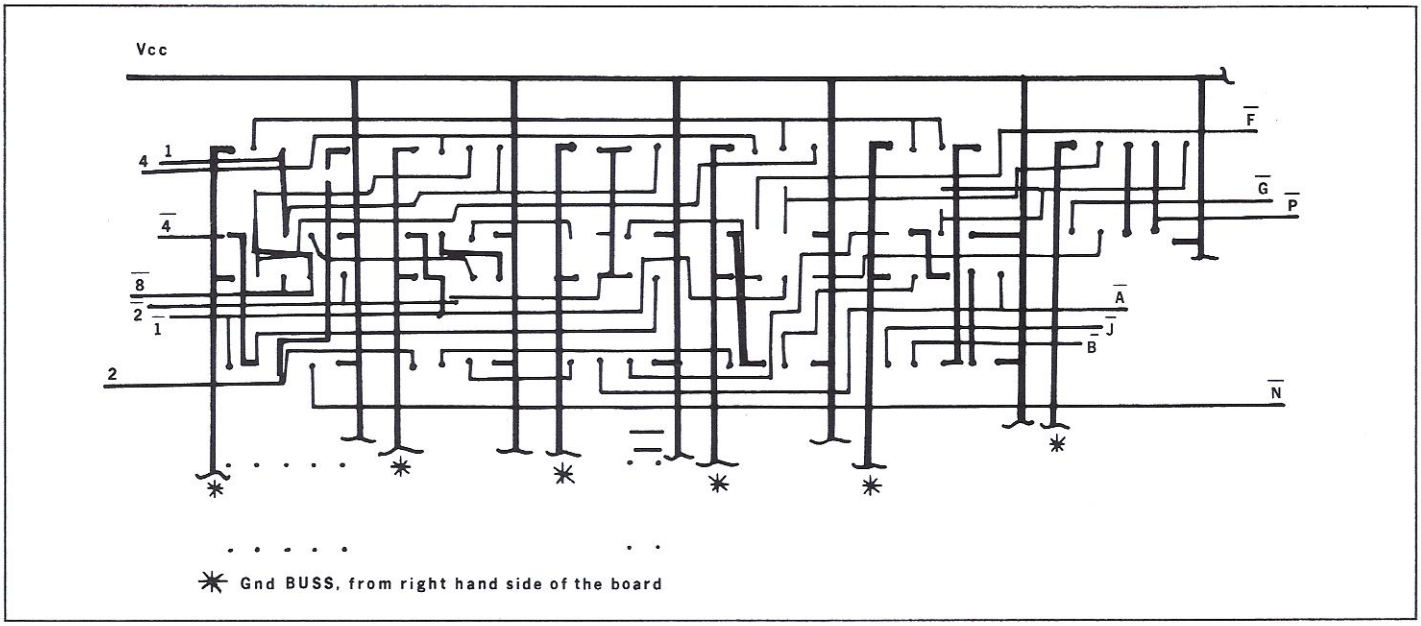

Fig. 6. Example of Printed-Circuit Layout Sheet.

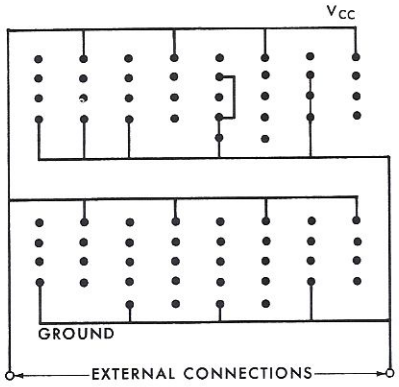

Fig. 7. A Typical Example of Horizontal, V_{CC}, and Ground Conductor Patterns.

Taping

Sheets of "Mylar" or K&E tracing cloth are reliable materials to tape onto. Place a sheet securely over the layout and tape the fingers and the pads. A problem with two-sided PC boards is proper registration of one side to the other. An aid in registration is Color Key.* In using this method, pads and fingers are taped on one sheet only. The sheet is then placed on a sheet of light-sensitive Color Key, with the emulsion side face down on a light box. After being exposed for 2 to 3 minutes, the Color Key is turned emulsion side up and 3M developer applied. The resulting negative is used by the same process to make two positives. Your tape masters will now be in good registration. Grid pattern overlays may be used with this process.

Fig. 8a is a positive (1X) of a taped artwork reduced 2X, taken in part from the circuit shown in Fig. 6. The negative in Fig. 8b is another example of grid matrix techniques using the dual-in-line configuration.

*3M Company, Part No. 5PE-411.

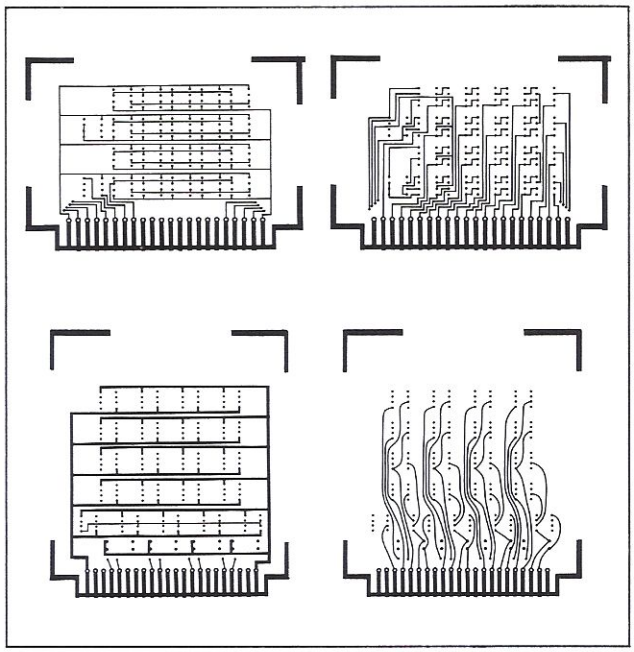

Fig. 8. Completed Printed-Circuit Board Artwork.

Pattern Comparisons

At this point we have finished artwork. A simple layout will show the advantages of using grid patterns. Fig. 9 depicts three different procedures for implementing the same circuit. Fig. 9a is a dual-in-line grid pattern. This is a clear example of basically vertical and horizontal but discretely intermingled board sides. Note that all runs are quite direct, and that no through pins are required. Fig. 9b shows the wiring required for a circular pattern layout of the same circuit. The result is a larger area, more conductors, six through pins (compared to none previously) and a visual path that is more difficult to follow. Fig. 9c shows the same cir-

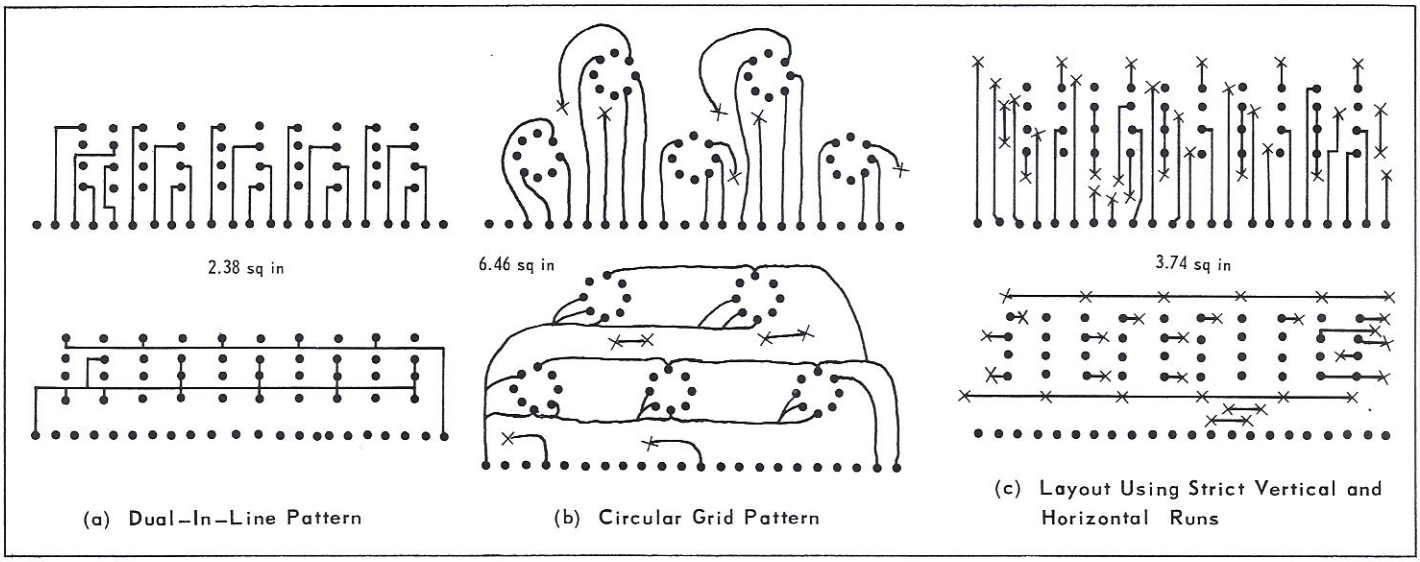
2.38 sq in
6.46 sq in
3.74 sq in
(a) Dual-In-Line Pattern
(b) Circular Grid Pattern
(c) Layout Using Strict Vertical and Horizontal Runs

Fig. 9. Comparison of Line Run Techniques.

cuit laid out in a dual-in-line pattern, but using strictly horizontal and vertical sides. The X's indicate through pins required (3). The circuit is difficult to follow, and the number of drilled holes required on the board is almost doubled. Note that nine additional points were given the benefit of the doubt and curved into the pad rather than using through pins.

The first time one comes in contact with the grid matrix system there is a tendency to discount the system for various reasons. Some of these reasons are: the use of smaller than usual lines and spaces; the capability of conductor runs between the lead pads; and the not uncommon problem of becoming familiar with a new technique. This reluctance has been evident in both customer assists and by comments in various publications and presentations. An excellent example of this is a comment made by a reader of this paper as originally published. The reader suggested an alternate method for laying out the circuit, shown here as Fig. 9b. The intention of Fig. 9 is to show that the dual-in-line grid matrix configuration, using a basically horizontal side and a basically vertical side (9a), is superior to the pin circle configuration in density, simplicity, and lack of through-holes (9b) and to the strictly horizontal and vertical side (9c). This suggested alternate used a similar amount of room as Fig. 9b but was still twice the size of Fig. 9a. Additionally, the circuit chosen for comparison was extremely simple, but a restriction was placed on the location of the external connectors to increase the complexity and to add further proof of the advantage of method 9a. The external connections were previously set as if, perhaps, the board was an IC replacement for a previously discrete component board, without disturbing the board-to-board interconnections. In this particular case, all through-holes were eliminated, but the circuit was kept identical by using the method shown in Fig. 9a. The suggested alternate using the pin circle configuration eliminated the through holes but altered seven external pin connections

TABLE II.

PC BOARD DIMENSIONAL CHART.

PC BOARD (actual size)		100-mils center to center, 300-mil row	50 mils	20 mils	25 mils
GRID SPACING	TO-5-8 pin	●			
	TO-5-10 pin	●			
	DIP-14 pin	●			
	DIP-16 pin	●			
PAD SIZES	TO-5-8 pin		●		
	TO-5-10 pin		●		
	DIP-14 pin		●		
	DIP-16 pin		●		
LINE WIDTH AND SPACING	Minimum			●	
	Maximum		●		
	Typical				●

Once one becomes familiar with dual-in-line grid matrix schemes, implementing circuits is easy and the advantages become obvious.

A review of the discussions of the dimensions for pads, lines, and spaces is shown in Table II.

Artwork to Completed Board

The bulk of the job is completed, and one of several paths may be followed to complete the PC board, as shown in Fig. 10. Since much has already been written on this subject, only two basic possibilities will be discussed.

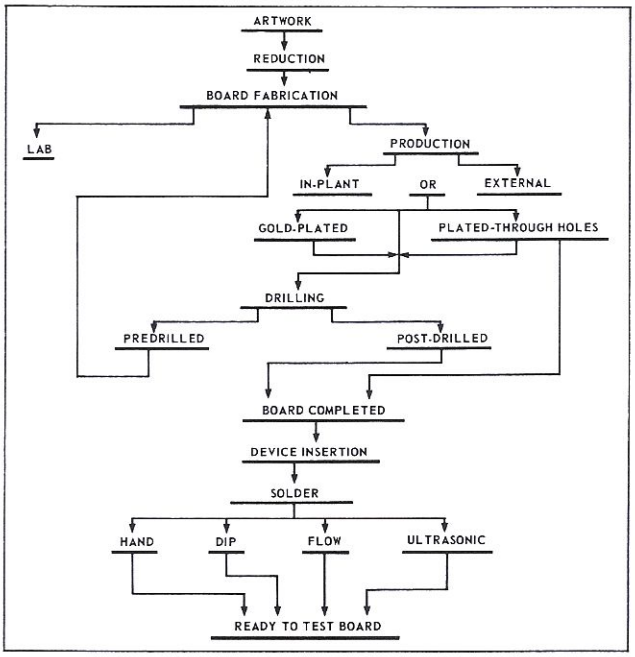

Fig. 10. Multipossibility Chart for Completing PC Board from Artwork.

Method One-If the PC board is a prototype, and if a lab area is available, a satisfactory and usable board may be built. After the artwork has been reduced, select a board and follow these four simple steps:

1. Apply photoresist.
2. Expose on the light box.
3. Develop in TCE vapor.
4. Etch in ferric acid.

The board then is drilled, stuffed, soldered, and ready to test.

Method Two-If a production PC board is required, the following various steps can be taken, depending on the circumstances.

1. Board may be goldplated.
2. Plated-through holes may be used.
3. Board may be pre-drilled or post-drilled. Various methods of drilling may be used, from one to many boards, from machine drill to a special drilling machine

4. Soldering may be by hand, hand dip, machine dip, wave or flow, fountain, or ultrasonic.

SUMMARY

Using the basic principles we have discussed, a logic circuit design may be accurately converted with relative ease first into PC artwork, then into a PC board, and finally into a functional part of a system. Utilizing "Systematic Procedures," the method can be summarized into goals and steps, as outlined below.

Goals

1. Logical implementation must be easy.
2. Tooling for prototypes must be simple and tooling for high-volume production inexpensive.
3. Visual checks must be simple at all states of progress; i. e., design, layout, manufacture, and test.
4. Finally, the method should tend to look or "feel" wrong if it is, in fact, wrong.

Steps Used

1. The system spec is developed. ICP's are chosen and any special circuits required are developed.
2. Logical design is completed and functional groups are emphasized.
3. Logic and power supply interconnections are developed by using a 2X scale pencil layout, working on a matrix of basically horizontal and vertical runs.
4. Taping of the 2X scale artwork from the layout is checked against the logical design.
5. Photographic reduction to actual size is made from which two-sided PC boards are fabricated.
6. ICP's are inserted and soldered, and the function is tested. Any correction made to the board is also made on the design and artwork.

Use of "Systematic Procedures" both in the applications and in R&D areas has shown that the number of errors in each step is sufficiently negligible to open the possibility of eliminating breadboarding. At the moment, large boards that are slightly modified for the final PC boards have been designed for breadboard stages. These possibilities are discussed in detail in References 5 and 6.

Useful Construction Aids

1. Gummed transparent overlays of logic symbols and/or grid patterns.
2. Grid matrix pattern.
3. Single dual-color, layout sheet.
4. Color Key to aid side-to-side registration.
5. Location layout sheet to correlate between the artwork/printed-circuit board and the logic/system schematic.
6. Insertion techniques.

REFERENCES

1. Rex Rice, "Systematic Procedures for Digital System Realization from Logic Design to Production"; reprinted from the Proceedings of the IEEE; Vol. 52, No. 12; December 1964.
2. Murray Siegel, "System Applications and Packaging Techniques for Microcircuits"; presented on mid-western trip; April 6-9, 1965.
3. J. Irwin, "Implementation of Integrated Circuits in Systems"; presented at the IEEE Section at Rochester, N. Y. ; April 9, 1965.
4. J. Irwin, "Answering Some Unanswered Questions"; Electronic Design; May 24, 1965; p. 62.
5. Rex Rice, "Functional Design and Interconnections Key to Inexpensive Systems"; Fairchild Semiconductor publication; 1965.
6. Jerry Tennant and Chesley Gilman, "Design and Layout of Large Integrated Circuit Boards"; Fairchild Semiconductor publication; 1965.

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